WHAT IS CLAIMED IS:

1. A process for producing a semiconductor device, which comprises forming a first insulation layer on a principal surface of a semiconductor substrate, depositing a silicon layer on the first insulation layer, depositing a first metallic layer on the silicon layer, depositing a metal nitride layer on the first metallic layer, depositing a second metallic layer on the metal nitride layer, etching a stacked structure of the silicon layer, the first metallic layer, the metal nitride layer and the second metallic layer and forming a gate electrode, doping an impurity onto the surface of the semiconductor substrate, on both sides of the gate electrode, using the gate electrode as a mask, annealing the gate electrode, and reacting the first metallic layer with the silicon layer, thereby forming a metal silicide layer between the metal nitride layer and the silicon layer.

2. A process according to Claim 1, wherein the annealing is carried out at 650°C or higher.

3. A process according to Claim 1, wherein the metal silicide layer is a tungsten silicide layer, the metal nitride layer is a tungsten nitride layer, and the first and second metallic layers are tungsten layers.

4. A process according to claim 1, wherein the silicon layer is doped with an impurity.

5. A process according to claim 1, wherein the silicon layer is a polycrystalline silicon layer.

6. A process according to claim 1, wherein the reaction of the first metallic layer with the silicon layer during annealing is such that the metal silicide layer is formed to have a thickness of about twice as large as the deposited first metallic layer.

7. A process for producing a semiconductor device, which comprises forming a first insulation layer on a principal surface of a semiconductor substrate, depositing a silicon layer on the first insulation layer, depositing a first metallic layer on the silicon layer, depositing a metal nitride layer on the first metallic layer, depositing a second metallic layer on the metal nitride layer, annealing a stacked layer comprising the silicon layer, the first metallic layer, the metal nitride layer and the second metallic layer and reacting the first metallic layer with the silicon layer, thereby forming a metal silicide layer between the metal nitride layer and the silicon layer, etching the stacked layer and forming a gate electrode, and doping an impurity onto the surface of the semiconductor substrate on both sides of the gate electrode, using the gate electrode as a mask.

8. A process according to Claim 7, wherein the annealing is carried out at 650°C or higher.

9. A process according to Claim 7, wherein the metal silicide layer is a tungsten silicide layer, the metal nitride layer is a tungsten nitride layer and the first and second

metallic layers are tungsten layers.

10. A process according to claim 7, wherein the silicon layer is doped with an impurity.

11. A process according to claim 7, wherein the silicon layer is a polycrystalline silicon layer.

12. A process according to claim 7, wherein the reaction of the first metallic layer with the silicon layer is such that the metal silicide layer is formed to have a thickness of about twice as large as the deposited first metallic layer.

13. A process for producing a semiconductor device, which comprises forming a first insulation layer on a principal surface of a semiconductor substrate, depositing a silicon layer on the first insulation layer, depositing a metal silicide layer on the silicon layer, depositing a metal nitride layer on the metal silicide layer, depositing a metallic layer on the metal nitride layer, etching the stacked layer comprising the silicon layer, the metal silicide layer, the metal nitride layer and the metallic layer, and forming a gate electrode, and doping an impurity onto the surface of the semiconductor substrate on both sides of the gate electrode, using the gate electrode as a mask.

14. A process according to Claim 13, wherein the metal silicide layer is a tungsten silicide layer, the metal nitride layer is a tungsten nitride layer and the metallic layer is a tungsten layer.

15. A process according to claim 13, wherein the silicon layer is doped with an impurity.

16. A process according to claim 13, wherein the silicon layer is a polycrystalline silicon layer.